## AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

**Listing of Claims:**

1. (currently amended) A processor comprising:

a queue configured to store one or more ~~instructions to be issued~~ entries identifying a cache miss, the one or more entries including a destination register field to identify a destination register associated with the cash miss and a tag associated with each destination register field to identify a fill corresponding to a cache miss for an entry; and

a control circuit coupled to the queue, wherein the control circuit is configured to detect a replay of an instruction in a load/store pipeline due to a load miss, and wherein the control circuit is configured to enter into a stall state and inhibit issuance of instructions to the load/store pipeline, the control circuit to couple a destination register value to the queue associated with the load miss, in which the queue is to respond with a fill tag associated with the destination register, the control circuit to store the fill tag in a miss tag register and to compare the fill tag in the miss tag register with fill tags of fill data being returned, wherein when a returned fill tag matches the fill tag in the miss tag register, the load/store pipeline exits the stall state~~and to one or more other pipelines by comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss, until fill data in response to the load miss is returned for loading, the control circuit further includes a storage device to store a miss tag corresponding to the destination register of the instruction causing the load miss and to compare the stored miss tag to a fill tag that is sent to the control circuit when fill data is returned, in which when the miss tag and the fill tag match, the control circuit to exit the stall state to start issuing instructions from the queue to the pipelines~~.

2. (previously presented) The processor as recited in claim 1 wherein the control circuit is configured to inhibit issuance of the instructions until fill data is provided to a data cache of the processor.

3. (canceled)

4. (currently amended) The processor as recited in claim 2 wherein the control circuit further includes a comparator coupled to the ~~storage device~~ miss tag register to compare the fill tag in the miss tag register to ~~the~~ fill tags of returned fill data to determine if the fill data being returned corresponds to the load miss.

5. (currently amended) The processor as recited in claim 2 wherein multiple ~~load~~ cache misses may be present in which comparison of the miss tag register and ~~the~~ fill tags identifies fill data to its corresponding load miss.

6-9. (canceled)

10. (currently amended) The processor as recited in claim 2 wherein the control circuit is configured to permit issuance ~~of one of the~~ of one or more instructions if one or more instructions lack dependency to the load miss.

11. (previously presented) The processor as recited in claim 10 wherein dependencies to the load miss are maintained by one or more scoreboards coupled to the control circuit.

12. (previously presented) The processor as recited in claim 11 wherein the control circuit is configured to detect dependencies on the load miss using one or more scoreboards which track instructions that have passed a stage of a pipeline where replay is signaled.

13. (canceled)

14. (currently amended) A method comprising:

detecting a replay of a first instruction due to a dependency on a load miss in a load/store pipeline of a processor;

comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss;

inhibiting issuance of one or more instructions from a queue to the load/store pipeline and to one or more other pipelines of the processor responsive to detecting the replay of the load/miss in the load/store pipeline by entering a stall state;

sending a destination register value to a queue that stores an entry identifying the load miss, the entry including a destination register field to identify a destination register associated with the load miss and a tag associated with the destination register field of the load miss to identify a fill tag corresponding to the load miss;

returning the fill tag from the queue as a miss tag;

storing ~~a~~ the miss tag corresponding to the load miss in ~~response to detecting the replay~~ a register;

~~generating a fill tag when fill data corresponding to the load miss is returned~~

comparing ~~the~~ a fill tag of fill data being returned to the miss tag to identify when fill data corresponding to the load miss is being returned; and

exiting the stall state to allow one or more instructions to issue to the pipelines ~~after comparing the fill tag and the miss tag results in a match~~ when a fill tag of fill data matches the miss tag.

15. (previously presented) The method as recited in claim 14 wherein exiting the stall state to allow one or more instructions to issue occurs after fill data is provided to a data cache.

16-17. (canceled)

18. (currently amended) The method as recited in claim 15 wherein multiple load misses may be present in which comparing the miss tag and ~~the~~ fill tags identifies fill data to its corresponding load miss.

19-22. (canceled)

23. (currently amended) The method as recited in claim 15 further comprising permitting issuance ~~of one of the~~ of one or more instructions if one or more instructions lack the dependency to the load miss.

24. (previously presented) The method as recited in claim 23 further comprising detecting lack of dependency for an instruction in one or more scoreboards.

25. (previously presented) The method as recited in claim 23 further comprising detecting lack of dependency for an instruction by checking one or more scoreboards which track instructions that have passed a stage of the pipeline where replay is signaled.

26. (canceled)

27. (currently amended) A computer accessible medium comprising one or more data structures to manufacture a processor, the processor including:

a queue configured to store one or more ~~instructions to be issued~~ entries identifying a cache miss, the one or more entries including a destination register field to identify a destination register associated with the cash miss and a tag associated with each destination register field to identify a fill corresponding to a cache miss for an entry; and

a control circuit coupled to the queue, wherein the control circuit is configured to detect a replay of an instruction in a load/store pipeline due to a load miss, and wherein the control circuit is configured to enter into a stall state and inhibit issuance of instructions to the load/store pipeline, the control circuit to couple a destination register value to the queue associated with the load miss, in which the queue is to respond with a fill tag associated with the destination register, the control circuit to store the fill tag in a miss tag register and to compare the fill tag in the miss tag register with fill tags of fill data being returned, wherein when a returned fill tag matches the fill tag in the miss tag register, the load/store pipeline exits the stall state ~~and to one or more other pipelines by comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss, until fill data in response to the load miss is returned for loading, the control circuit further includes a~~

~~storage device to store a miss tag corresponding to the destination register of the instruction causing the load miss and to compare the stored miss tag to a fill tag that is sent to the control circuit when fill data is returned, in which when the miss tag and the fill tag match, the control circuit to exit the stall state to start issuing instructions from the queue to the pipelines~~.